REMARKS

The above amendments and following remarks are submitted under 37 C.F.R. 1.116 in response to the Final Official Action of the Examiner mailed November 3, 2005. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

Applicants object to the finality of the pending rejection. Even though the Examiner states at paragraph 19:

> Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

This statement is clearly erroneous, because claims 21-25 have never been amended and yet are finally rejected on entirely new grounds. Claims 21-25 had previously been rejected under Applicants' Admitted Prior Art (AAPA) in view of Hazawa (as to claim 21) and further in view of Lynch (as to claim 22) and further in view of Lai (as to claims 23-25). Claims 21-25 now stand finally rejected in view of new combinations all based upon the newly cited Abato reference, even though claims 21-25 have never been amended. Clearly the final rejection of at least claims 21-25 is premature.

Claim 1 has been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,627,993, issued to Abato et al (hereinafter referred to as "Abato") in view of U.S. Patent No. 5,564,035, issued to Lai (hereinafter referred to as "Lai").

This ground of rejection is respectfully traversed as to amended claim 1 for failure of the Examiner to present a *prima facie* case of obviousness as specified by MPEP 2143.

In alleging motivation to combine Lai with Abato, the Examiner improperly concludes that motivation exists, because the prior art exists. The Examiner states:

> Since (sic) the technology ..... was well known.....an atisan would have been motivated....

Not only does this conclusion fly in the face of controlling law, it does great injustice to the definition of the verb, "to motivate". The Examiner has simply failed to meet his burden of showing motivation. The Examiner completely ignores his obligation to show reasonable likelihood of success. As a result, the Examiner has failed to make two of the three showings required of MPEP 2143.

Furthermore, amended claim 1 is limited by a "semi-store-in" level one cache memory and associated tag memory which are not found in the alleged combination. The rejection of amended claim 1, and all claims depending therefrom, is respectfully traversed.

Claims 2-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato in view of Lai and further in view of U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). This ground of rejection is respectfully traversed for the reasons provided below.

Applicants have provided substantial previous arguments concerning the lack of showing of motivation and lack of showing of reasonable likelihood of success of the alleged combination as required by MPEP 2143. To the untenable, unmotivated, and not likely to succeed combination of Abato and Lai, the Examiner fails to motivate the alleged further combination with Lynch. He again improperly concludes:

> Since (sic) the technology.....was well known.....an artisan would have been motivated....

This statement is clearly erroneous in addition to being improper as a matter of law.

Furthermore, claims 2-4 depend from amended claim 1, which is deemed patentable for the reasons provided above. Claims 2-4 are each limited by unique limitation which have been discussed at length in previous responses. For example, claim 2 is limited by "second logic" which inhibits invalidation under certain conditions. This is not found in the prior art of record. The rejection of amended claim 2 is respectfully traversed.

Similarly, claim 3 requires a "third logic" which is not found in the prior art of record. The rejection of amended claim 3 is respectfully traversed.

Claim 4, as amended, is further limited by "fourth logic which records location of data within the level one cache memory". Notwithstanding the Examiner's citation of extensive material from Lai, this feature is simply not in the prior art of

record. The Examiner has not met his obligation of MPEP 2143 to show "all claimed elements" within the alleged combination and finds the claim obvious. The rejection of claim 4 is respectfully traversed.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato in view of Lynch and further in view of Lai and further in view of U.S. Patent No. 4,891,809, issued to Hazawa (hereinafter referred to as "Hazawa"). This ground of rejection is respectfully traversed for the following reasons.

Claim 5 depends from claim 4 and is further limited by a "Fifth logic which detects a parity error in said level two cache memory and which in response invalidates said corresponding level one cache memory location[1] to avoid loss of control between said level one cache memory and said level two cache memory". In other words, the claimed "fifth logic" detects and invalidates a memory location in response thereto. In making his rejection, the Examiner cites Hazawa column 3, lines 38-48, which does not detect but generates a "pseudo-error" in accordance with column 3, line 26.

Furthermore, the most that Hazawa can do about such a "pseudo-error" (or perhaps even an actual parity error) is set

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[1]The Examiner never uses the term "memory location" but instead states that Hazawa invalidates "a level one cache memory" in his rejection leading one to suspect that he has confused the claimed single memory location with the entire memory. The practical significance of this distinction should be readily apparent.

one of "error indicating flags" 45, 46, 47, or 48. None of these "error indicating flags" can specify the location of an error, but can only indicate that an error has occurred (i.e., been generated as a "pseudo-error") somewhere in the memory. The alleged combination cannot meet the limitations of claim 5. Though these issues have been previously pointed out to the Examiner, he continues to ignore Applicants' invention as claimed preferring to reject claim 5, as if it were rewritten to further comport with his preconceived rejection. Surely he can distinguish between indication of a parity error at a particular location of a cache memory as claimed and indication of a parity error at some unspecified location within a cache memory as shown by Hazawa. The rejection of claim 5 is respectfully traversed.

Claims 6 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato in view of Lai and further in view of U.S. Patent No. 6, 128,711 issued to Duncan et al (hereinafter referred to as "Duncan"). This ground of rejection is respectfully traversed.

Claim 6 as amended has six individual major elements. The alleged combination does not have all of these major elements and in particular does not have the claimed "system controller" or either element e. or element f. The rejection of claim 6, and all claims depending therefrom, is respectfully traversed.

Claim 9, as amended, depends from claim 8, which depends from claim 7, which depends from 6 and is further limited by a "fourth logic" which performs the recording of an invalidated location. As a result, the alleged combination admittedly does not contain all of the limitations of claim 9. Furthermore, the alleged combination has no "fourth logic" as claimed. The rejection of claim 9 is respectfully traversed.

Claims 7 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato in view of Lai and further in view of Duncan and further in view of Lynch. Because the Examiner presents no legally cognizable motivation, ignores the requirement to show reasonable likelihood of success, and does not show all of the claimed elements, this ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato, in view of Lai, further in view of Duncan, and further in view of Hazawa. This ground of rejection is respectfully traversed.

Claim 10, as amended, depends from claim 9. Therefore, the alleged combination admittedly does not meet all of the limitations of amended claim 10.

In addition to the issues raised above concerning the claims from which claim 10 depends, the alleged combination does not

have circuitry which invalidates a "corresponding portion" of the level one cache memory. In fact, the Examiner does not even consider the claimed elements. Instead, he states:

> Hazawa discloses **invalidating a level one cache memory** in response to a level two cache memory generating a parity error (col. 3, lines 38-48). (emphasis added)

This finding is clearly erroneous, because Hazawa shows only generation of a "pseudo-error" by Diagnostic Unit 1. There is no parity error generated by Cache Memory Unit 2. The Examiner's statement is also legally irrelevant, because it does not address the claimed invention. The Examiner discusses invalidating the entire level one cache memory. This is not claimed. The rejection of claim 10 is respectfully traversed.

Claims 11, 14, 16, and 19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Duncan and further in view of U.S. Patent No. 6,128,711, issued to Arimilli et al (hereinafter referred to as "Armilli"). This ground of rejection is respectfully traversed as to the amended claims.

Claim 11 is a method claim having four basic steps. It requires an environment having a "semi-store-through level one cache memory", "system controller", "tag memory" and "duplicate tag memory". These elements are important to the operation of the method. None of the other prior art of record has any of these claimed elements. Therefore, in addition to the lack of showing of motivation to make the allege combination and lack of

showing of reasonable likelihood of success of the alleged combination, the rejection of amended claim 11, and all claims depending therefrom, is respectfully traversed[2].

Claim 14, as amended, depends from claim 13 and is therefore admittedly not obvious over the alleged combination. Furthermore, claim 14 is further limited by three additional steps including "recording location of data corresponding to said read memory request within said level one cache memory" wherein the record of location of the data must be made within the level one cache memory. None of the prior art of record meets these limitations. The rejection of claim 14 is respectfully traversed.

Claim 16 has been amended to require that the level one caching means is "semi-store-through" and that the level two caching means and level one storing means are located within a "system controller". These limitations are fully supported in the specification. The rejection of claim 16, and all claims depending therefrom, is respectfully traversed.

Claims 12-13 and 17-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Duncan and further in view of Arimilli and further in view of Lynch. This

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[2]Arimilli is particularly incompatible in that it requires a "write through" interface as specifically excludes "partial-write" through (see column 6, lines 36-38.

ground of rejection is respectfully traversed for the reasons discussed below.

It seems clear that the Examiner has alleged a completely untenable combination of four, mutually incompatible references in an attempt to find the words from Applicants' claims, without providing the legally mandated attention to the claimed invention.

Each of these claims depend from either amended claim 11 or amended claim 16 which are deemed patentable over the alleged rejection for the reasons presented above. The embodiment of Lai relied upon by the Examiner for his rejection of claims 11 and 16 is the fully inclusive prior art example shown at Fig. 3 of Lai. One would not combine that embodiment with Lynch to add the claimed limitations of claims 12-13 and 17-18 because such additions would be superfluous. Lai has no mode 3 with ownership, because this would make no sense in the applied architecture of Lai which employs full inclusion of level one cache memory in level two cache memory. The Examiner continues to mix architectures in ways which do not make any sense. Similarly, Lai has no need for the claimed elements of claims 13 and 18. The fully inclusive architecture chosen by the Examiner does not and cannot utilize these elements. The rejection of claims 12-13 and 17-18 is respectfully traversed.

Claims 15 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Duncan and further in view of Arimilli and further in view of Hazawa. This ground of rejection is respectfully traversed for the reasons provided below.

Both claims 15 and 20 require detection of a parity error. Hazawa only shows generation of a "pseudo-error". There is no disclosure of an actual parity error or structure in response thereto. Furthermore, claim 15 requires invalidation of a "portion" of the data, whereas claim 20 requires invalidation of an "element". Hazawa does not invalidate any particular portion or element. It simply sets a flag with regard to the entire cache memory wherein an error is generated. With Hazawa, one cannot distinguish between whether there is a single byte containing a parity error or whether the entire cache memory is inoperative. Again, the Examiner ignores the claimed invention stating:

> Hazawa discloses **invalidating a level one cache memory** in response to a level two cache memory generating a parity error (column 3, lines 38-48) (emphasis added)

Furthermore, the Examiner continues to ignore the claimed requirement that a **level two** parity error invalidates a portion of the **level one** cache memory. There is no showing that Hazawa does anything by indicate a parity error in the directly

associated memory. The rejection of claims 15 and 20 is respectfully traversed.

Claim 21 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato in view of Hazawa. This ground of rejection is respectfully traversed.

Claim 21, as amended, requires "a data element having a parity error stored in said level two cache memory" and "a facility which detects said parity error of said data element and invalidates a corresponding data element within said level one cache memory". The alleged combination does not have these elements. Perhaps acknowledging this lack of teaching, the Examiner states:

> Hazawa discloses invalidating data in a level two cache memory in response to a parity error of a data element to provide a cache memory with an error checking mode [col. 3, lines 38-51; col. 3, lines 38-59].

This statement ignores both the clear language of Applicants' claims and the clear teaching of Hazawa. Hazawa shows no "data element having a parity error" and no invalidation of a "corresponding data element". Furthermore, the claim requires invalidation of a single data element. Hazawa has no way to determine the location of any particular parity error. The rejection of claim 21 is respectfully traversed.

Claim 22 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato, in view of Hazawa, and further in view of Lynch. This ground of rejection is respectfully traversed.

In addition to the issues raised with regard to claim 21 from which claim 22 depends, the alleged combination does not have the additional claim elements. Therefore, the rejection of claim 22 is respectfully traversed.

Claims 23-25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Abato, in view of Hazawa, further in view of Lynch, and further in view of Lai. This ground of rejection is respectfully traversed because the Examiner has again alleged the combination of incompatible architectures for the purpose of adding superfluous functionality as explained in detail above. The rejection of claims 23-25 is respectfully traversed.

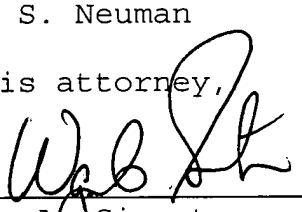
Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

Paul S. Neuman

By his attorney,



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